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QUANTUM REALIZATION OF TERNARY ADDER CIRCUITS

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ABSTRACT

Ternary quantum circuits have recently been introduced to realize ternary logic functions. In this paper realizations of ternary half- and full-adder circuits using generalized ternary gates (GTG) are proposed, which are more efficient than the previously published realizations.

1. INTRODUCTION

Quantum computing (QC) is a very promising and flourishing research area [1-3]. QC theoretically allows designers to build much more efficient computers than the existing classical ones. For example, some problems that cannot be solved in polynomial time using classical computers can be solved in polynomial time using quantum computers [1]. In part, this is because quantum circuits are inherently able to perform massive parallel computations [1-3]. While most of the results are for binary quantum computers, the multiple-valued quantum logic synthesis is a very new research area. Unfortunately, previous synthesis methods produce circuits that were unnecessarily complex.

The success in the ion trap quantum realization of some ternary gates [4] gives increasing hopes to physically build complete ternary quantum circuits in this or other quantum realization technologies. However, even when the ternary quantum technology will become available, synthesizing automatically a quantum circuit from its specification is not a trivial problem and most previous attempts have been disappointing or insufficient from one point of view or another. Another issue is the quantum realizability of gates and their costs. Some authors [5-9] assume complex gates that are not directly realizable in quantum. The costs of realizing these gates using realizable gates from [4] would be very high. Only two-qudit (*qu*antum *dig*it) gates are directly realizable [4] and other gates are compositions of realizable gates. Paper by Muthukrishnan and Stroud [4] introduced families of realizable 2-qudit controlled gates in which only one value, the highest one, can be controlling. That means, for all but the highest value of the controlling variable the data variable (controlled variable) is unaffected. Otherwise a ternary 1-qudit operation is done on the controlled variable. Based on the understanding of paper [4], the ***generalized ternary gates*** (GTG) are proposed in [10], where every value of the controlling variable can be used to select a ternary 1-qudit operator on the controlled variable. The matrices of such gates are unitary. It can be shown [11] that every GTG can be built from Muthukrishnan/Stroud gates [4]. In this paper we present realizations of ternary half- and full-adder circuits using GTG gates.

The rest of the paper is organized as follows. In Section 2, we describe the generalized ternary gate (GTG). Section 3 presents realization of ternary half- and full-adder circuits. Finally, in Section 4, we conclude the paper.

2. THE GENERALIZED TERNARY GATE

Six 1*1 ***ternary Shift gates*** are proposed in [9]. Operations and symbols of these gates are shown in Fig. 1, where the addition and multiplication are over Galois Field 3 (GF3). The ***Generalized Ternary gate (GTG)*** is proposed in [10] as shown in Fig. 2. Here, input A is the controlling input and input B is the controlled input. The output P is equal to the input A. The controlling input A controls a conceptual ternary multiplexer (a conditional gate) that can be realized using quantum technology such as ion traps [4]. If $A=0$, then the output Q is the x shift of the input B. Similarly, if $A=1$, then the output Q is the y shift of the input B and if $A=2$, then the output Q is the z shift of the input B. Here shift means all ternary shift operations including the Buffer (simple quantum wire). Readers should note that depending on the six possible Shift gates for each of the three positions of x, y, and z, there are $6^3 = 216$ possible GTGs. As the Conditional gate and the Shift gates are realizable in quantum technology, the GTGs are truly realizable ternary quantum gates.

Gate Name	Gate Symbol with operaton*
Buffer	x — x
Single-Shift	x — ' — $x' = x+1$
Dual-Shift	x — " — $x'' = x+2$
Self-Shift	x — ''' — $x''' = 2x$
Self-Single-Shift	x — # — $x^{\#} = 2x+1$
Self-Dual-Shift	x — ^ — $x^{\wedge} = 2x+2$

* Addition and multiplication are over GF3.

Fig. 1 Ternary Shift operations.

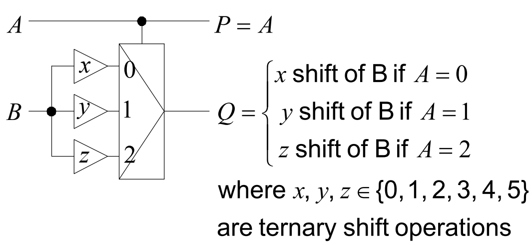

Fig. 2 Generalized Ternary Gate.

3. REALIZATION OF TERNARY ADDER CIRCUITS

The truth table of the ternary half-adder function is shown in Table 1. The realization of the ternary half-adder circuit using cascade of GTGs is shown in Fig. 3, where signal values of all intermediate signals are shown as map for verification of the correctness of the circuit.

The truth table of the ternary full-adder function is shown in Table 2. The realization of the ternary full-adder circuit using cascade of GTGs is shown in Fig. 4, where signal values of all intermediate signals are shown as map for verification of the correctness of the circuit.

Table 1: Truth table of ternary half-adder.

AB	$C_{out}S$
00	00
01	01
02	02
10	01
11	02
12	10
20	02
21	10
22	11

Table 2: Truth table of ternary full-adder.

ABC_{in}	$C_{out}S$
000	00
001	01
002	02
010	01
011	02
012	10
020	02
021	10
022	11
100	01
101	02
102	10
110	02
111	10
112	11
120	10
121	11
122	12
200	02
201	10
202	11
210	10
211	11
212	12
220	11
221	12
222	20

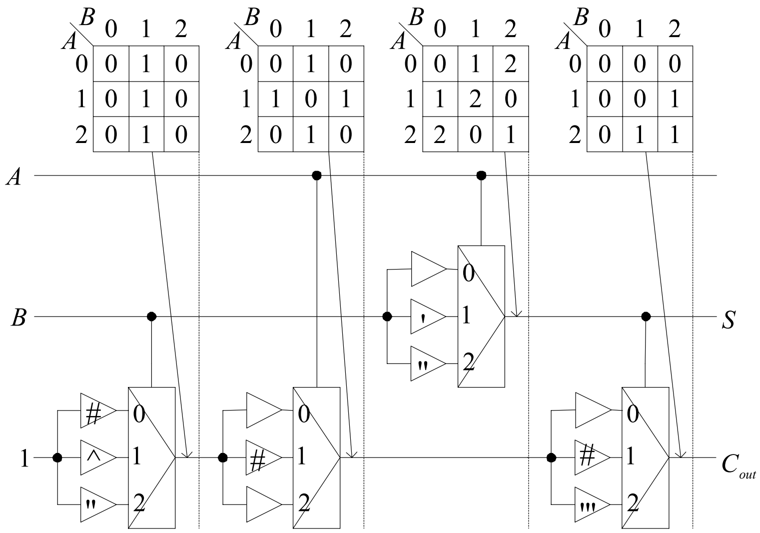

Fig. 3 Realization of ternary half-adder.

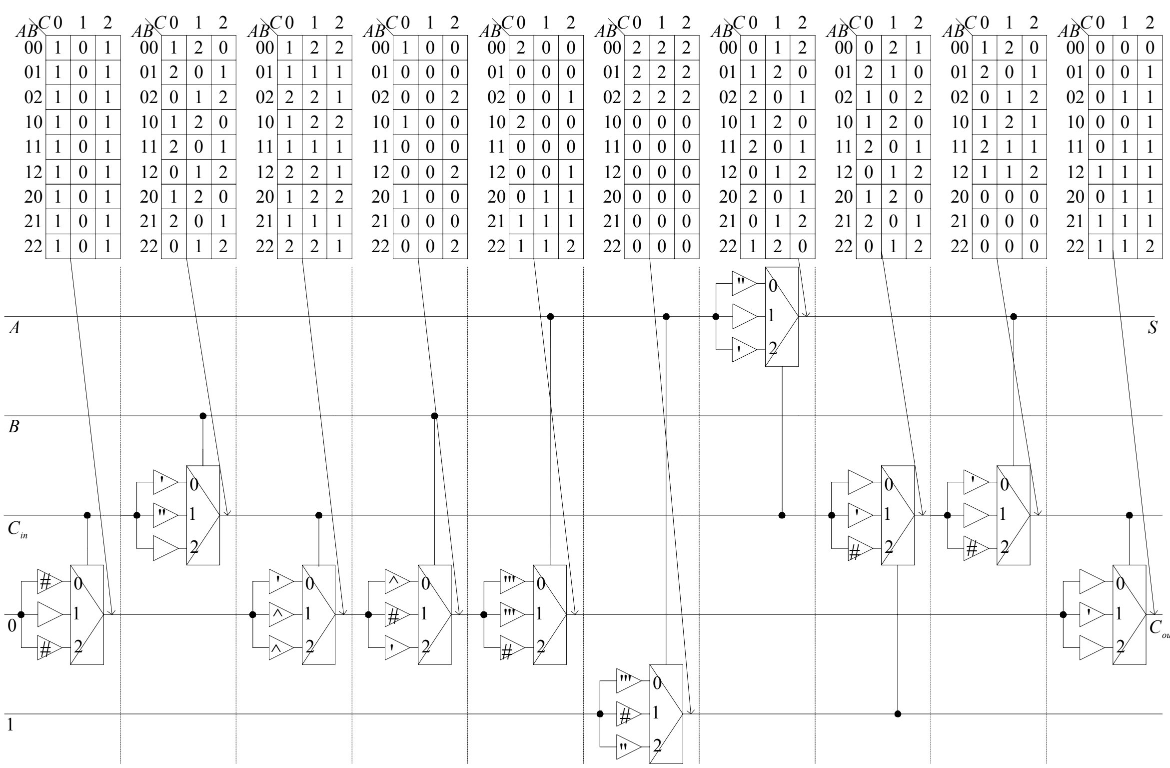

Fig. 4 Realization of ternary full-adder.

4. CONCLUSIONS

GTGs were proposed in [10] without giving any synthesis algorithm to synthesize from all these gates directly. In this paper we show realization of ternary half- and full-adder circuits using cascade of GTGs. The implementation of the ternary full-adder circuit of [7] requires four 4*4 gates, eight 3*3 gates, and four 2*2 gates totaling 16 gates. On the other hand, our ternary full adder circuit requires only 10 2*2 gates. In general, any $m*m$ ($m > 2$) gate is very difficult to realize in quantum technology, since interaction of more than two particles is nearly impossible to control. Therefore, these gates should be realized from 1*1 and 2*2 gates. Considering this fact, our solution is better than the solution from [7]. The ternary half-adder circuit is realized for the first time and, therefore, cannot be compared with other results.

REFERENCES

[1] M. Nielsen and I. Chuang, Quantum Computation and Quantum Information., Cambridge University Press, 2000.

[2] M. Hirvensalo, Quantum Computing., Springer Verlag, 2001.

[3] C. P. Williams and S. H. Clearwater, Explorations in Quantum Computing., Springer-Verlag, 1998.

[4] A. Muthukrishnan and C. R. Stroud, Jr., "Multivalued logic gates for quantum computation," Physical Review A, vol. 62, no. 5, pp. 052309/1-8, 2000.

[5] A. Al-Rabadi, Novel Methods for Reversible Logic Synthesis and Their Application to Quantum Computing, Ph. D. Thesis, PSU, Portland, Oregon, USA, 2002.

[6] A. Al-Rabadi and M. Perkowski, "Multiple-Valued Galois Field S/D Trees for GFSOP Minimization and their Complexity," in Proc. 31st IEEE Int. Symp. on Multiple-Valued Logic, Warsaw, Poland, pp. 159-166, 22 –24 May 2001.

[7] D. M. Miller, G. Dueck, and D. Maslov, "A Synthesis Method for MVL reversible logic," in Proc. 34th IEEE Int. Symp. On Multiple-Valued Logic, Toronto, Canada, pp. 74-80, 19-22 May 2004.

[8] E. Curtis and M. Perkowski, "A Transformation Based Algorithm for Ternary Reversible Logic Synthesis using Universally Controlled Ternary Gates," in Proc. IWLS 2004, Tamecula, California, 2-4 June 2004.

[9] M. H. A. Khan, M. A. Perkowski, and P. Kerntopf, "Multi-Output Galois Field Sum of Products Synthesis with New Quantum Cascades," in Proc. 33rd IEEE Int. Symp. On Multiple-Valued Logic, Tokyo, Japan, pp. 146-153, 16-19 May 2003.

[10] M. Perkowski, A. Al-Rabadi, and P. Kerntopf, "Multiple-Valued Quantum Logic Synthesis," in Proc. of 2002 International Symposium on New Paradigm VLSI Computing, Sendai, Japan, pp. 41-47, 12-14 Dec. 2002.

[11] N. Denler, B. Yen, M. Perkowski, and P. Kerntopf, "Synthesis of Reversible Circuits from a Subset of Muthukrishnan-Stroud Quantum Multi-Valued Gates," in Proc. IWLS 2004, Tamecula, California, 2-4 June 2004.