

## A NEW ULTRA-WIDEBAND TRANSCEIVER ARCHITECTURE FOR ON-CHIP WIRELESS INTERCONNECT

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### ABSTRACT

This paper describes a new system architecture for a proposed ultra-wideband radio transceiver. Targeting on-chip wireless interconnect design using CMOS technology, the radio can be used for intra-chip or inter-chip data communication at 250 kbps with processing gain of 36 dB. A narrow pulse (approximately 1 ns wide) is used as the basic signal component; spreading the energy over a gigahertz of bandwidth. The transmitter consists of a programmable UWB pulse generator, and an antenna and the receiver consists of an antenna, low noise amplifier, synchronizing circuit, and a detection unit. All the design concepts were simulated by MATLAB and the validity was confirmed.

### 1. INTRODUCTION

Conventional interconnect systems using metal are projected to be limited in their ability to meet the future interconnect needs [1]. To address this problem, inter-chip and intra-chip wireless interconnects using microwaves are being evaluated. Wireless interconnect systems are not only feasible to integrate into CMOS ICs but also provide an additional means for global communications, freeing up conventional wires for other uses.

In this paper, we propose a transceiver architecture to be used as wireless interconnect system by ultra-wideband (uwb) technology. UWB technology is generally defined as any wireless transmission scheme that occupies fractional bandwidth of more than 0.25. The fractional bandwidth is given by equation 1.

$$B_f = 2 \frac{f_H - f_L}{f_H + f_L} \quad (1)$$

where  $f_L$  = lower and  $f_H$  = higher -3dB point in spectrum respectively.

Gaussian monopulses and doublets are widely used for UWB systems owing to their desirable shapes of the spectrum and existence of simple closed loop expressions [2]. Figure 1 shows a Gaussian monopulse in the time domain and frequency domain.

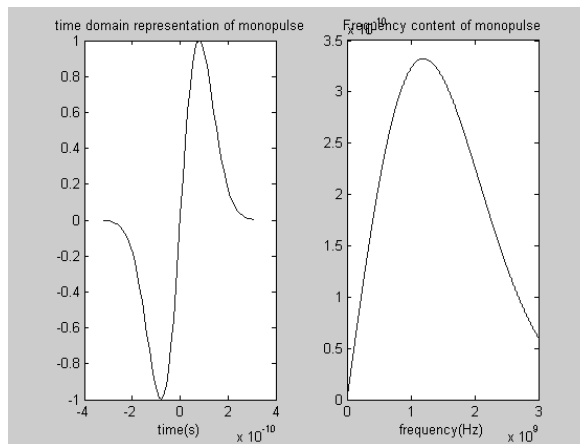


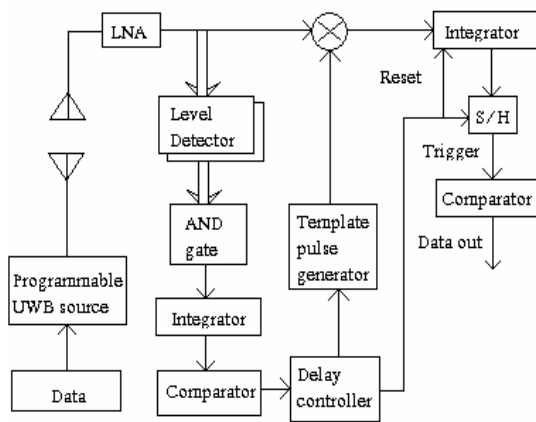
Fig. 1 Gaussian monopulse in the time domain and frequency domain.

A very wide bandwidth means better multipath mitigation, interference mitigation by using spread spectrum techniques, more users and high data rate [3]. A lower center frequency for a given bandwidth allows better material penetration. UWB system has no carrier. Therefore carrierlessness and very wide bandwidth makes

UWB technology as an attractive competitor in wireless interconnect system design.

The following sections introduce the proposed architecture along with pulse generation scheme, synchronization and data detection method. MATLAB simulation results of the whole transceiver are presented with each section.

## 2. SYSTEM OVERVIEW



**Fig. 2** Block diagram of the proposed transceiver

Figure 2 is a simplified block diagram of the proposed transceiver. Following chapters explain the details of each part.

### 2.1 Transmitter:

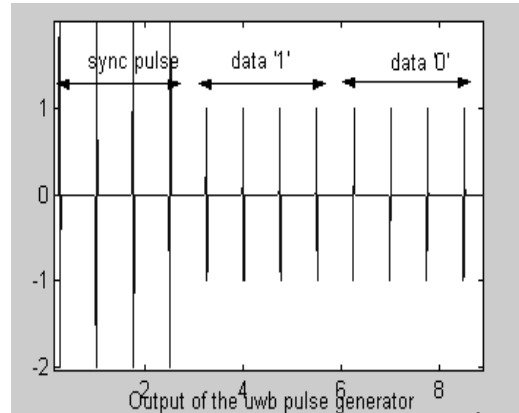
A programmable UWB source with the facility to generate both positive and negative Gaussian monopulses of two different amplitude levels is used as the pulse generator [4].

The data scheme is such that four consecutive monopulses are treated as a single unit to represent a data bit. For '1', all the pulses in the block are positive monopulse and for '0', all of them are negative monopulse as shown in figure 3.

### 2.2 Receiver:

In the receiver, the signal is first amplified by a Low Noise Amplifier (LNA) [5]. Its main function is to provide enough gain to overcome the noise of subsequent stages. In other words, LNA gives signal

amplification, without any degradation of signal to noise ratio (SNR).

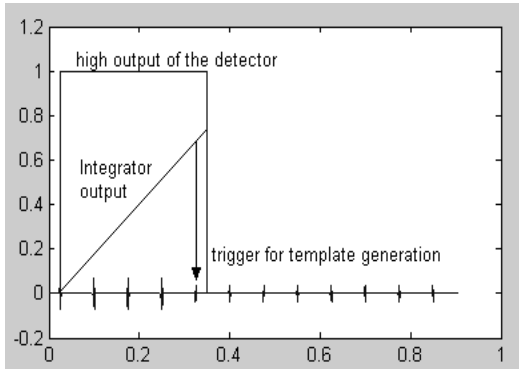


**Fig. 3** Output of the programmable UWB source, pulses being modulated by data.

### 2.2.1 Synchronization:

In ultra-wide band communication, synchronization is one of the most significant problems because of the very short impulses. In our proposed method, in order to maintain synchronization, special synch pulses are interleaved between the data pulses and transmitted to the receiver. Same as data scheme, synch pulses comprise of four consecutive monopulses, each having twice the magnitude of the data pulses. Unlike '1' or '0', synch monopulses are alternately positive and negative in order to differentiate it from the data pulses during detection period.

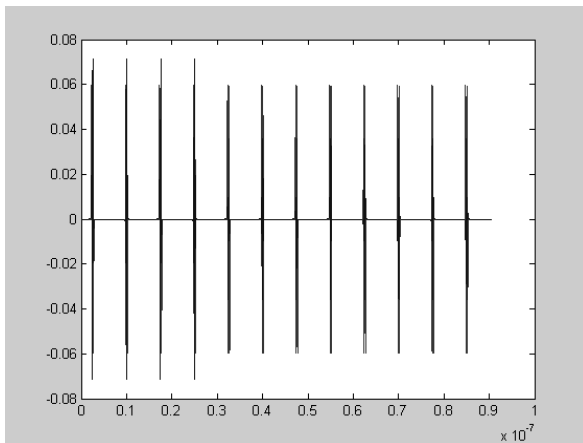
After the LNA, the received signal is fed to the level detectors which provide high output if the signal crosses a threshold level. There are two of them, one for detecting the positive peak and the other is for sensing the negative peak of the synch pulse and thus an AND gate following the detectors can ensure the arrival of a synch pulse if both the detectors provide high output. This bipolar synch pulse detection scheme can prevent data pulses to trigger the synchronizing unit in a noisy environment. The pulses generated by the detectors remain high for one time duration of monopulse repetition. The integrator following the detectors generates a ramp output whenever synch pulses arrive and when it reaches a threshold level, the comparator is used to provide reset and trigger pulses to the data detection unit through a proper delay controller. The synchronizing process is illustrated in figure 4.



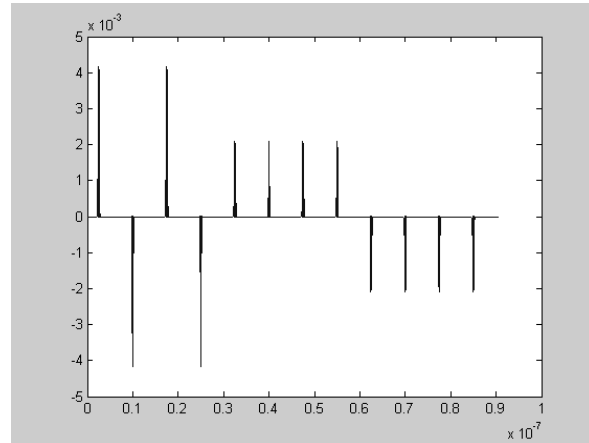
**Fig. 4** Synchronizing process

### 2.3 Data detection:

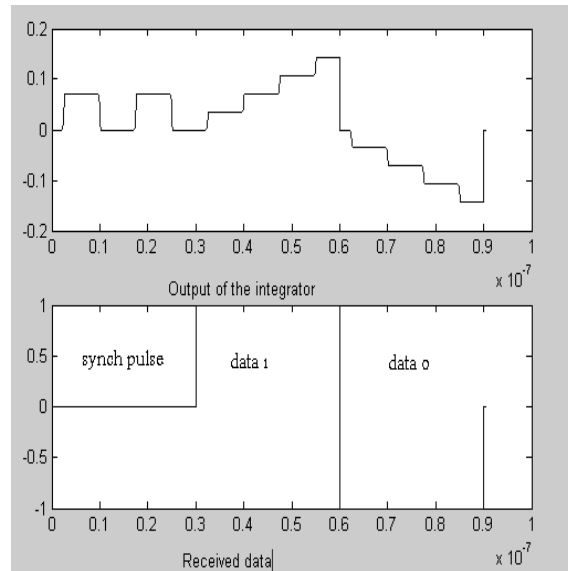
The data detection scheme in our proposed architecture is as simple as possible. The delay controller provides appropriate timing information of the monopulses in the data stream to the template pulse generator. In our simulation, we used a sinusoidal template pulse to cross-correlate with the data pulses (figure 5). The cross-correlation is realized by a multiplier followed by an integrator. If the arrived data is '1', the multiplication of the data pulses with the template pulse provides all positive outputs and hence the output of the integrator is above a positive threshold level. Similarly, if the arrived data is '0', the multiplication provides all negative outputs and hence the output of the integrator is below a negative threshold level. For synch pulse blocks, monopulses are alternately positive and negative and hence the output of the integrator is zero (figure 6). Now a sample and hold circuit triggered by the delay controller is used to sample the integrator output and finally a bipolar logic comparator is used to provide data output.



**Fig. 5** template pulse superimposed on received signal



**Fig. 6** Output of the multiplier



**Fig. 7**(a) output of the integrator in data detection unit (b) received data

## CONCLUSION

In this paper, we described hardware design concept for ultra-wide band on-chip wireless interconnect system and proposed a new simplified receiver architecture. The simplification is achieved in terms of simplified synchronizing circuit which requires simple blocks such as comparator, AND gate, integrator and counters. The noise margin of the data detection scheme is designed to improve by using blocks of four pulses to represent one bit as well as by using bipolar scheme of data detection. In order to improve the performance, the high period of the level detector can be doubled so that proper

synchronization is maintained even if any synchronizing pulse is somehow missed.

Topics for further work are, determination of an effective channel model in the presence of multipath and noise, increase in data rate by using m-ary modulation schemes and an evaluation of inter frame and inter frame interference that limits channel capacity.

### REFERENCES

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