3rd International Conference on Electrical & Computer Engineering
ICECE 2004, 28-30 December 2004, Dhaka, Bangladesh

FAULT CHARACTERIZATION AND TESTABILITY ISSUE OF LOW CAPACITANCE FULL-SWING BiCMOS LOGIC CIRCUITS

Hamidur Rahman[1]*, M. Faisal*[2] *and A. B. M. H. Rashid*[3]

Department of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology, Dhaka-1000, Bangladesh
E-mail: [1]hamidurrahman@eee.buet.ac.bd, [2]mohfaisa@eee.buet.ac.bd, [3]abmhrashid@eee.buet.ac.bd

ABSTRACT

Behavior of low capacitance full-swing BiCMOS logic gate under various single stuck faults has been investigated in this paper. Results show that more than 65% stuck-on faults in logic circuits can be detected by monitoring the power supply current popularly known as I_{DDQ} testing, but no logic monitoring is possible. Stuck-open faults in the logic MOS devices are detectable by logic monitoring using appropriate two-pattern test but stuck-open faults in the bipolar drivers are masked by the additional MOS devices used to attain full output logic swing.

1. INTRODUCTION

BiCMOS technology emulates CMOS technology in speed and current driving capability [1]~[5]. BiCMOS technology is attracting increasing interest for high-speed VLSI circuits as it combines the high-speed performance of Bipolar with the low power consumption of CMOS circuits. But conventional BiCMOS circuits do not have full output logic swing due to base-emitter voltage drop in the bipolar drivers. This shortcoming is mitigated by adding extra MOS devices as clamping diodes at the output. However, the resulting full-swing BiCMOS circuits have high output node capacitance. An alternative full-swing circuit has been proposed which gives much lower output capacitances [6]~[8]. Fault analysis of various classes of BiCMOS logic circuits has been reported [9]~[12]. S. M. Aziz *et. al.* [13] have shown that the stuck-open faults are masked in low capacitance full swing BiCMOS logic gates. But the fault characterization and testability of this class of BiCMOS circuits have not yet been analyzed fully. This paper investigates the behavior of BiCMOS logic circuits under different single stuck fault and also addresses the testability issue.

2. FAULT ANALYSIS OF BiCMOS LOGIC CIRCUITS

2.1 Fault Modeling: Physical defects may occur in ICs during manufacturing process, which may cause fault during use. BiCMOS technology combines Bipolar and CMOS devices on a single substrate, so this type of IC is more prone to defects. Most of the defects found in BiCMOS integrated circuits can be broadly categorized as shorts and opens. First type of defect causes stuck-on fault and the second type causes stuck-open fault in BiCMOS circuits. In this paper, these types of defects are modeled and simulated using SPICE simulator. The following two faults are studied:

Stuck-on Fault: If a transistor is permanently ON irrespective of the input signal applied at the gate then it is referred to as *stuck-on*. This fault may occur when the source and drain terminals of a transistor (emitter and collector in case of BJT) are short-circuited due to mask misalignment or excessive source-drain out diffusion etc. This type of fault can be modeled by placing a resistance R_f that indicates fault strength in parallel with the transistor between the respective terminals as shown in Figure 1(a). The value of R_f depends on the strength of the defect. In our analyses the fault strength is assumed to be less than 10 kΩ for stuck-on fault.

Stuck-open Fault: Physical defects or electromigration in aluminum conductor may cause a MOS transistor to become permanently open and insensitive to its input signal. A transistor is said to be *stuck-open* if it cannot be brought into conduction by applying any input signal. To model a stuck open fault a large resistance greater than 10 MΩ is inserted between the device terminal and the circuit node to which the terminal would otherwise be connected as shown in Figure 1(b).

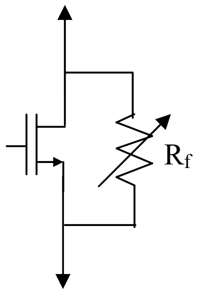

Fig. 1(a) Stuck-on fault model for MOS device

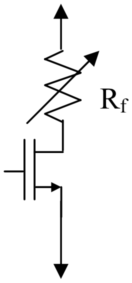

Fig. 1(b) Stuck-open fault model for MOS device

Single stuck-open fault can be detected by applying two-pattern test, the first vector to be applied is called initialization vector and the second vector is called test vector [14], [15]. Two vectors are applied to the faulty circuit sequentially. These two vectors are chosen so that under faulty condition, at first the initialization vector is applied in such a fashion that the faulty MOS will not be activated. Then the test vector sensitizes the fault in such a manner that the faulty MOS activates. In a fault free circuit the output node is supposed to change its logical state. However due to the fault the output may hold its previous state. In that case the fault will be detectable by logic monitoring.

2.2 BiCMOS Logic Circuits: Low capacitance full swing BiCMOS NAND and NOR gates are shown in Figure 2 and 3 respectively. Node 1 and 2 are input nodes and 5 is output node for both gates. The behavior of these circuits is first simulated under defect free conditions. Then fault is introduced in each of the devices and behavior of these circuits for various single stuck-on and stuck-open faults has been analyzed. The qualitative analysis and SPICE simulations have been done for every single stuck fault. SPICE 0.35 micron CMOS level-3 parameters are used for MOS devices and Gummel-Poon model parameters for bipolar transistors. The fault strength for all cases is varied from 0 to 10 kΩ for stuck-on fault and 10 MΩ to 100 MΩ for stuck-open fault. Maximum normal operating current is about 60 pA. A capacitive load of 1 pF is used for BiCMOS circuits.

Stuck-on fault in mp_5 ($dsmp_5$): Consider that the pMOS transistor mp_5 in Figure 2 is stuck on. This fault is sensitized for any one of the input vectors <00>, <01>, and <10>. Thus when at least one of the input vectors is 0, the node 4 is charged towards

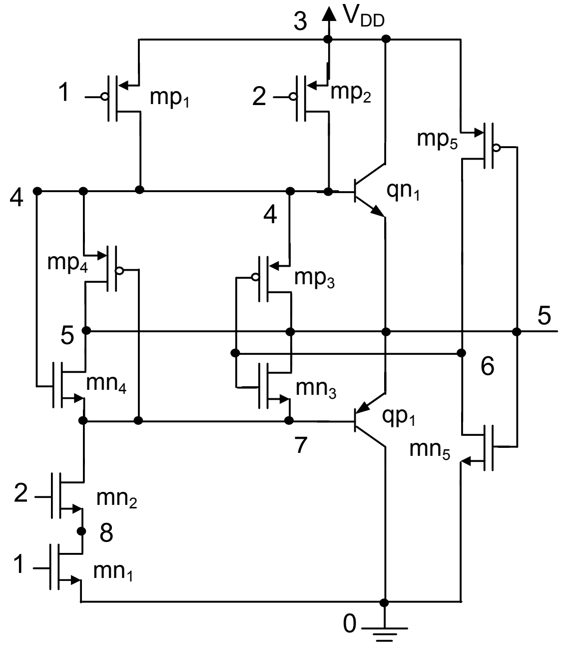

Fig. 2 Low capacitance full-swing BiCMOS NAND gate

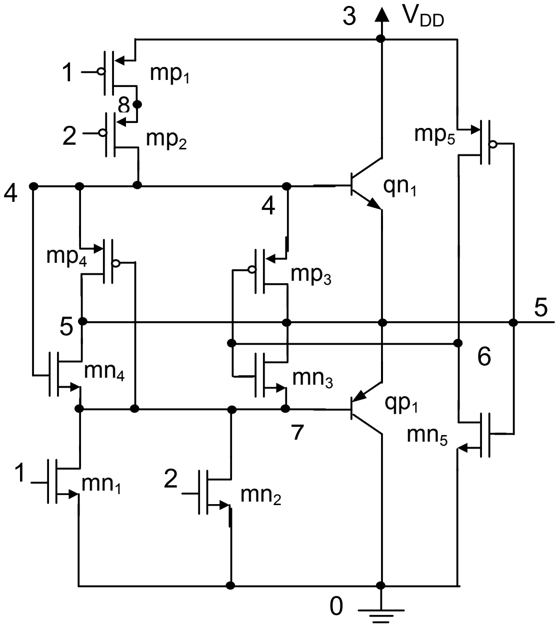

Fig. 3 Low capacitance full-swing BiCMOS NOR gate

V_{DD} through that ON pMOS. This turns on the BJT qn$_1$ ON and charges V_5 to ($V_{DD} - V_{BE}$). So mn$_5$ turns ON and a low resistance path exists between V_{DD} and ground through faulty transistor mp$_5$ and ON transistor mn$_5$. As a result power supply current increases in the range of 0.93-0.42 mA when the fault strength varies from 1 Ω to 10 kΩ whereas the maximum normal operating current is about 60 pA. So the current increment is about 10^7 times and the fault may be detected by current monitoring. However, the voltage at V_6 depends upon the fault strength R_f and may vary from 0.829V to 4.999V.

The correct voltage level at V_6 is supposed to be 0V. At this voltage mp$_3$ would be ON and raise V_5 to full swing output of $V_{DD} = 5V$. If V_6 shows an incorrect high logic level due to fault then full swing output voltage is not obtained since then mp$_3$ is OFF and mn$_3$ is ON. MOS mn$_4$ operates in a normal fashion and clamps qp$_1$ OFF. Since the output shows correct logic level so it may not be detected by logic monitoring at the output node.

Stuck-on fault in mn$_1$ (dsmn$_1$): Let us assume that the nMOS transistor mn$_1$ in Figure 3 is stuck on. The fault is sensitized for the input vector <00>. For this input both pMOS logic transistors are ON. So node 4 is charged towards V_{DD} through these series transistors. This turns ON the BJT transistor qn$_1$ and charges output node. Since the nMOS transistor is stuck ON so there exists a low resistance path between node 7 and ground and node 7 discharges towards ground potential. Therefore qp$_1$ is also ON. So output node charges through qn$_1$ and discharges through qp$_1$ simultaneously. As a result the power supply current increases in the range of 87.53 –24.01 mA depending on the fault strength whereas the maximum normal operating current is about 60 pA. The gate to source voltage of mn$_4$ and mp$_4$ is greater than the threshold voltage. So these transistors are also ON providing another current path from V_{DD} to ground. The node voltage V_4 depends on the ON resistances of mp$_1$, mp$_2$, mp$_4$, mn$_4$ and the fault strength at mn$_1$. As a result the output voltage is indeterminate. The fault therefore cannot be detected by logic monitoring. As the increment in power supply current is 10^8 times the normal operating current so the fault may be detected by current monitoring. The variation in power supply current I_{DDQ} and output node voltage V_5 for different fault strength has been demonstrated in Figure 4.

Stuck-on fault in qn$_1$ (ceqn$_1$): Consider that the bipolar transistor qn$_1$ in Figure 3 is stuck on. The fault may be observed when the input vectors are any one of <01>, <10> and <11>. For <01> input, mn$_1$ is OFF and mn$_2$ is ON. So node 7 is discharged to 0 V through transistor mn$_2$. This turns ON bipolar transistor qp$_1$. So output voltage is discharged through transistor qp$_1$ and at the same time it is charged through the faulty transistor qn$_1$. The output voltage depends on the fault strength and may vary from 4.91–1.18 V. So the voltage level V_5 is indeterminate and therefore logic monitoring is not possible. Since qp$_1$ is ON and qn$_1$ is stuck on so a low resistance path exists between V_{DD} and ground. The power supply current varies from 90.31 –0.42 mA depending on the fault strength. The current increases at least by 10^7 times and hence I_{DDQ} testing is possible.

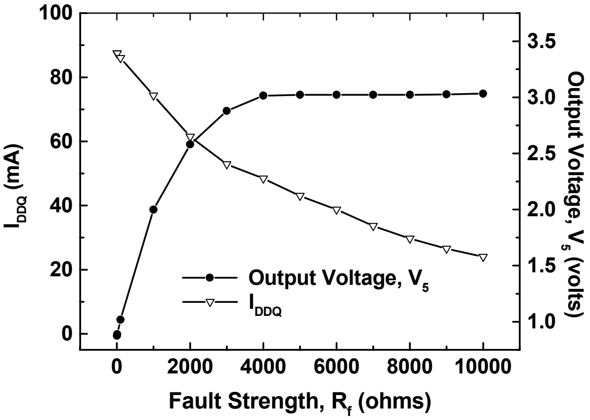

Fig. 4 Variation of output voltage and power source current I_{DDQ} for stuck-on fault dsmn$_1$ in low capacitance full-swing BiCMOS NOR gate for the test vector <00>

Similar analysis and SPICE simulations have been carried out for single stuck-on fault for other devices. The simulation results for stuck-on fault for all transistors of each of the gates are summarized in Table 1.

Stuck-open fault in mn$_3$ (dmn$_3$): Assume that the MOS mn$_3$ is stuck open in Figure 2. Two-pattern test is necessary to sense the fault in this MOS. Initially one of the input vectors <00>, <01> and <10> is applied so that the output rises to high logic level. Now the input is changed to <11>. So node 7 is discharged to 0 V through transistor mn$_1$ and mn$_2$. This turns ON the pnp transistor qp$_1$ and V_5 discharges to V_{BEp} through qp$_1$. The output inverter feeds the inverted voltage back to V_6. Since mn$_3$ is stuck open so V_5 cannot attain the full swing voltage of 0 V rather it discharges upto about 0.75 V. The power supply current changes from 44 pA to 108 μA when input vector switches from initialization to fault sensitization vector, whereas in a fault-free circuit the current changes from 45 pA to 274.03μA. Therefore the fault cannot be detected either by logic monitoring or current monitoring.

Table 1: Simulation results for Stuck-on fault

Fault	NAND		
	Test vector <V_1V_2>	V_5 Volts (Output voltage)	I_{DDQ}
dsmp$_1$	<11>	4.15-2.63	57.49-21.17mA
dsmn$_1$	<01>	3.02-3.35	76.72-21.27mA
ceqp$_1$	<00><01><10>	0.20-4.13	200-0.43mA
ceqn$_1$	<11>	4.94-1.64	61.6-0.44mA
dsmp$_3$	<11>	0	45pA
dsmn$_3$	<00><01><10>	5	37pA
dsmp$_4$	<00><01><10>	5	44pA
dsmn$_4$	<11>	0	45pA
dsmp$_5$	<00><01><10>	4.99-5	0.93-0.42mA
dsmn$_5$	<11>	0.13-0	2.14-0.47mA
	NOR		
dsmp$_1$	<10>	3.02-2.03	76.74-26.28mA
dsmn$_1$	<00>	0.88-3.03	87.53-24.01mA
ceqp$_1$	<00>	0.09-3.46	94.11-0.55mA
ceqn$_1$	<01><10><11>	4.91-1.18	90.31-0.42mA
dsmp$_3$	<01><10><11>	0	40pA
dsmn$_3$	<00>	5	42pA
dsmp$_4$	<00>	5	53pA
dsmn$_4$	<01><10><11>	0	40pA
dsmp$_5$	<00>	4.99-5	0.93-0.42mA
dsmn$_5$	<01><10><11>	0.13-0	2.14-0.47mA

Stuck-open fault in qp$_1$ (cqp$_1$): Two-pattern test is applied to sensitize the stuck-open fault in the bipolar transistor qp$_1$ shown in Figure 3. For fault sensitizing an initial input vector of <00> is applied to achieve an output voltage of 5V. Now an input vector of <01>, <10> or <11> is applied to activate the fault. If <10> is applied at the input transistor,

Table 2: Simulation results for stuck-open fault

Fault	NAND		
	Test vector <V_1V_2>	V_5 (Output voltage)	I_{DDQ}
smp$_1$	<11:01>	0:0.013V	45pA: 1.85nA
dmn$_1$	<00,01,10:11>	5:5V	44pA: 4.67nA
cqp$_1$	<00,01,10:11>	5:1.59V	44pA: 346μA
cqn$_1$	<11:00,01,10>	0:3.14V	45pA: 1.64mA
dmp$_3$	<11:00,01,10>	0:4.15V	45pA: 11.5mA
dmn$_3$	<00,01,10:11>	5:0.75V	44pA: 108μA
dmp$_4$	<00,01,10:11>	5:1.35V	44pA: 281μA
dmn$_4$	<11:00,01,10>	0:3.92V	45pA: 2.96mA
smp$_5$	<00,01,10:11>	5V:0.5V	44pA: 622nA
smn$_5$	<11:00,01,10>	0:4.28V	45pA: 665μA
	NOR		
smp$_1$	<01,10,11:00>	0:0.02V	40pA: 26nA
dmn$_1$	<00:10>	5:5V	53pA: 10nA
cqp$_1$	<00:01,10,11>	5:0.55V	53pA: 205μA
cqn$_1$	<01,10,11:00>	0:3.31V	40pA: 605μA
dmp$_3$	<01,10,11:00>	0:4.08V	40pA: 1.77mA
dmn$_3$	<00:01,10,11>	5:0.61V	53pA: 75μA
dmp$_4$	<00:01,10,11>	5:0.77V	53pA: 421μA
dmn$_4$	<01,10,11:00>	0:3.23V	40pA: 2.47mA
smp$_5$	<00:01,10,11>	5:0.57V	53pA: 41μA
smn$_5$	<01,10,11:00>	0:4.19V	40pA: 276μA

mn_1 is ON and discharges V_7 to 0 V. Since collector of qp_1 is open so V_5 cannot discharge through qp_1. Considering that V_4 is still at previous high logic level mp_4 and mn_4 are ON and discharges V_4 and V_5. When the output crosses the inversion voltage, V_6 goes to high logic level and mn_3 turns ON shunting the output to low voltage level. So the fault is not detectable by logic monitoring at the output. The power supply current changes from 53 pA to 205 μA when input vector switches from initialization to fault sensitization vector whereas in a fault-free circuit the current changes from 53 pA to 278 μA. So the fault is not detectable by current monitoring either. However, since BJTs are not involved during the transition from high to low logic level of output voltage, so the speed will be degraded for this fault.

Table 3: Summary for single stuck-on fault in low capacitance full-swing BiCMOS circuits
Logic Monitoring = LM, Current Monitoring = CM
Indeterminate = I, Correct = C

Fault	NAND			
	Output logic level	I_{DDQ} increment	LM	CM
$dsmp_1$	I	10^{8}	No	Yes
$dsmn_1$	C	10^{8}	No	Yes
$ceqp_1$	I	10^{7}	No	Yes
$ceqn_1$	I	10^{7}	No	Yes
$dsmp_3$	C	10^{0}	No	No
$dsmn_3$	C	10^{0}	No	No
$dsmp_4$	C	10^{0}	No	No
$dsmn_4$	C	10^{0}	No	No
$dsmp_5$	C	10^{7}	No	Yes
$dsmn_5$	C	10^{7}	No	Yes
	NOR			
$dsmp_1$	I	10^{8}	No	Yes
$dsmn_1$	I	10^{8}	No	Yes
$ceqp_1$	I	10^{7}	No	Yes
$ceqn_1$	I	10^{7}	No	Yes
$dsmp_3$	C	10^{0}	No	No
$dsmn_3$	C	10^{0}	No	No
$dsmp_4$	C	10^{0}	No	No
$dsmn_4$	C	10^{0}	No	No
$dsmp_5$	C	10^{7}	No	Yes
$dsmn_5$	C	10^{7}	No	Yes

Similar analysis and SPICE simulations have been carried out for single stuck-open fault for other devices. The simulation results for stuck-open fault for all transistors of each of the gates are summarized in Table 2.

Table 4: Summary for single stuck-open fault in low capacitance full-swing BiCMOS circuits
Logic Monitoring = LM, Current Monitoring = CM
Correct = C, Incorrect = Inc

Fault	NAND			
	Output logic level	I_{DDQ} increment	LM	CM
smp_1	Inc	10^{-4}	Yes	No
dmn_1	Inc	10^{-4}	Yes	No
cqp_1	C	10^{0}	No	No
cqn_1	C	10^{0}	No	No
dmp_3	C	10^{1}	No	No
dmn_3	C	10^{0}	No	No
dmp_4	C	10^{0}	No	No
dmn_4	C	10^{1}	No	No
smp_5	C	10^{-3}	No	No
smn_5	C	10^{0}	No	No
	NOR			
smp_1	Inc	10^{-4}	Yes	No
dmn_1	Inc	10^{-4}	Yes	No
cqp_1	C	10^{0}	No	No
cqn_1	C	10^{0}	No	No
dmp_3	C	10^{0}	No	No
dmn_3	C	10^{-1}	No	No
dmp_4	C	10^{0}	No	No
dmn_4	C	10^{1}	No	No
smp_5	C	10^{-1}	No	No
smn_5	C	10^{0}	No	No

3. CONCLUSION

Theoretical analysis and SPICE simulations of fault characterization and testability of low capacitance full swing BiCMOS circuits under various single stuck faults are presented in this paper. The final summary of simulation results is shown in Table 3 and 4. It is found that stuck-on faults in logic MOS transistors, Bipolar drivers and two additional MOS devices at the output inverter of each gate can only be detected by signal source current monitoring i.e. I_{DDQ} testing. The increment in current for stuck-on fault is normally assumed to be 10^6 times the normal operating current for detecting the fault. Stuck-open faults in logic MOS transistors are only detectable by logic monitoring using appropriate two-pattern test. Stuck-open faults in Bipolar drivers and additional MOS devices can be detected neither by logic monitoring nor by current monitoring.

4. REFERENCES

[1] Y. K. Tseng, and C. Y. Wu, "A new true-single-phase clocking BiCMOS dynamic pipelined logic family for high-speed, low-voltage pipelined system applications," *IEEE J. Solid-State Circuits*, Vol. 34, no. 1, pp. 68-79, Jan. 1999

[2] Y. K. Tseng, and C. Y. Wu, "A 1.5-V differential cross-coupled bootstrapped BiCMOS logic for low-voltage applications," *IEEE J. Solid-State Circuits*, Vol. 33, no. 10, pp. 1576-1579, Oct. 1998

[3] M. Margala, and N. G. Durdle, "Noncomplementary BiCMOS logic and CMOS logic for low-voltage, low-power operation-a comparative study," *IEEE J. Solid-State Circuits*, Vol. 33, no. 10, pp. 1580-1585, Oct. 1998

[4] S. H. Embabi, A. Bellaour, and M.I. Elmasry, "Digital BiCMOS Integrated Circuit Design," *Kluwer Academic Publishers*, USA, 1993

[5] A. R. Alvarez, "BiCMOS Technology and Applications," *Kluwer Academic Publishers*, 2nd Edn., USA, 1993

[6] S. M. R. Hasan, and C. D. Rajagopal, "Low-voltage dynamic BiCMOS CLA circuit with carry skip using novel full-swing logic," *IEEE J. Solid-State Circuits*, Vol. 32, no. 1, pp. 70-78, Jan. 1997

[7] H. J. Shin, "Full-Swing BiCMOS logic circuits with complementary emitter- follower driver configuration," *IEEE J. of Solid-State Circuits*, vol. 26, no. 4, pp. 578-584, 1991

[8] H. J. Shin, "Full-Swing complementary BiCMOS logic circuits," *Proc. IEEE Bipolar Circ. And Tech. Meeting*, pp. 229-232, Sept. 1989

[9] A. E. Salama and M. I. Elmasry, "Fault characterization, testing consideration, and design for testability of BiCMOS logic circuits," *IEEE J. of Solid State Circuits*, vol. 27, no. 6, pp. 944-947, 1992

[10] B. E. Stewart, D. Al-Khalili, and C. Rozon, "Defect modeling and testability analysis of BiCMOS circuits," *Canadian J. Elect. and Comp. Engg.*, vol. 27, pp. 944-947, 1992

[11] M. E. Levitt, K. Roy, and J. A. Abraham, "BiCMOS logic testing," *IEEE trans. VLSI Systems*, vol. 2, no. 2, pp. 241-247, 1994

[12] S. C. Ma and E. J. McCluskey, "Non-conventional faults in BiCMOS digital circuits," *Proc. IEEE Int. Test Conf.*, pp. 882-891, Oct. 1992

[13] S. M. Aziz and A. B. M. H. Rashid, "Fault masking in low capacitance full swing BiCMOS logic circuits," *J. of Elect. Engg.*, The Institution of Engineers, Bangladesh, vol. EE 25, no. I & II, 1997

[14] R. L. Wadsack, "Fault modeling and logic simulation of CMOS and MOS integrated circuits," *Bell Syst. Tech. J.*, vol. 57, no. 5, pp. 1449-1474, 1978

[15] W. Maly, P. K. Nag and P. Nigh, "Testing oriented analysis of CMOS ICs with opens," *Proc. Int. Conf.*, Computer-Aided Design, Santa Clara, CA, pp. 344-347